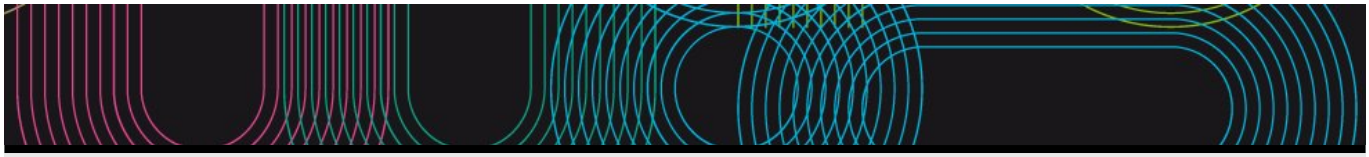

IDENTIFYING DATA				
Design and synthesis of digital systems				
Subject	Design and synthesis of digital systems			
Code	V05G300V01923			
Study programme	Degree in Telecommunications Technologies Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	4th	1st
Teaching language	English			
Department				
Coordinator	Álvarez Ruiz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo			
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General description	This course will be taught and assessed in English. The course documentation is in English. The main learning goals of this course are: □ Introduction to VHDL for synthesis. □ Design and synthesis of synchronous digital systems. □ Development, synthesis and verification of programmable digital circuits, using VHDL for its application in the field of the Telecommunications.			

Competencies

Code	
B1	CG1: The ability to write, develop and sign projects in the field of Telecommunication Engineering, according to the knowledge acquired as considered in section 5 of this Law, the conception and development or operation of networks, services and applications of Telecommunication and Electronics.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C62	(CE62/OP5) The ability to design and synthesize complex digital systems by hardware description language.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Learning outcomes

Expected results from this subject	Training and Learning Results		
To be able to distinguish the differences between the use of Hardware Description Languages for simulation and for synthesis.	B13	C62	
To deepen the understanding of synchronous digital design techniques using VHDL for synthesis.	B13	C62	
To acquire skills at designing complex synchronous digital systems using VHDL.	B1 B9 B13	C62	D4

Contents

Topic

LESSON 1 THEORY (2 h.). INTRODUCTION TO COMPLEX DIGITAL SYSTEM DESIGN AND SYNTHESIS.	1.1.- Introduction. 1.2.- Types of digital integrated circuits. Microprocessors. DSPs. ASICs. FPGAs. 1.2.1.- Comparative analysis. 1.3.- Field Programmable Gate Arrays (FPGAs). 1.4.- Complex application specific digital system design by means of FPGAs. 1.4.1.- Sequential processing systems. Operational unit. Control Unit. 1.4.2.- Continuous processing systems.
LESSON 2 THEORY (2 h.). ADVANCED DIGITAL SYSTEM DESIGN.	2.1.- Introduction. 2.2.- General rules for the design of digital systems. 2.2.1.- Hierarchical design. 2.2.2.- Technology independent design. 2.2.3.- Design timing. 2.2.4.- Design for reuse. 2.2.5.- Design for verificability. 2.2.6.- Design documentation. 2.3.- Intellectual Property (IP) cores.
LESSON 3 THEORY (2 h.). INTRODUCTION TO SYNTHESIS OF DIGITAL SYSTEMS DESCRIBED IN VHDL.	3.1.- Introduction. 3.2.- Definition of synthesis. Basic concepts on synthesis. 3.3.- Conversion of a VHDL description to real hardware. Differences between the original VHDL model and the result of the synthesis / implementation. Timing simulation model. 3.4.- Recommendations for the description in VHDL synthesisable of distinct types of circuits. 3.5.- Examples of synthesisable models of commonly used circuits.
LESSON 4 THEORY (6 h.). VHDL FOR SYNTHESIS. RESTRICTIONS.	4.1.- Introduction. 4.2.- IEEE standard for synthesis. 4.3.- Time sentences (□After□, □Wait□). 4.4.- Loops (□Loop□). Loops □generate□. 4.5.- □Real□ data type. Type conversion. 4.6.- Complex arithmetical operations. Division (□/□). 4.7.- Complex mathematical functions. (□Without□, □Cos□, □Log□). 4.8.- Two-dimensional matrices. (□Array□). 4.9.- Exercises of non- synthesisable models and equivalent synthesisable circuits.
LESSON 5 THEORY (2 h.). ARITHMETICAL CIRCUITS DESIGN IN VHDL.	5.1.- Introduction. 5.2.- Representation of binary numbers with decimal part. Fixed point. Floating point. 5.3.- Design of fixed point applications. 5.4.- Design of floating point applications. 5.5.- Implementation of arithmetical circuits in FPGAs.
LESSON 6 THEORY (4 h.). VHDL ADVANCED SENTENCES.	6.1.- Introduction. 6.2.- Libraries and packages. 6.3.- Access to files. 6.3.1.- Memory initialisation. 6.3.2.- Testbench stimuli. 6.4.- □Generic□ data type. Parameterisable circuits. 6.5.- Subprograms. 6.5.1.- Functions. 6.5.2.- Procedures. 6.6.- Conditional compilation.
LESSON 7 THEORY (1 h.). VERIFICATION OF COMPLEX DIGITAL SYSTEMS.	7.1.- Introduction. 7.2.- Verification through simulation. 7.2.1.- Signals. Delay models. Definition of □driver□. 7.2.2.- Design analysis and simulation. Simulation cycle. Delta delay. 7.2.3.- Recommendations for VHDL simulation. Examples. Testbench design. 7.2.4.- Differences between functional and timing simulation. 7.3.- Verification through timing analysis. 7.4.- Verification through test in a development board. 7.5.- Exercises.
LESSON 1 LABORATORY (4 h. TYPE B). PRACTICAL TUTORIAL OF DIGITAL SYSTEM DESIGN AND SYNTHESIS.	1.1.- Introduction. 1.2.- Basic digital system design in synthesisable VHDL. 1.3.- Testbench design in VHDL. 1.4.- Implementation of digital systems in FPGAs. 1.5.- Testing digital systems.

LESSON 2 LABORATORY (2 h. TYPE B). DIGITAL SYSTEM DEBUGGING. VIRTUAL LOGICAL ANALYSERS.	2.1.- Introduction. 2.2.- Xilinx virtual logical analyser. Chipscope core. 2.3.- Parameters of the Xilinx virtual logical analyser. 2.4.- Implementation of the Xilinx virtual logical analyser. 2.5.- Analysis of a digital system by means of the Xilinx virtual logical analyser.
LESSON 3 LABORATORY. (15 h. = 8 H. TYPE B + 7 h. TYPE C). DESIGN OF A MEDIUM-COMPLEXITY DIGITAL SYSTEM IN SYNTHESISABLE VHDL.	3.1.- Introduction. Task explanation. (2 h. TYPE B) 3.2.- Project based learning. Discussions on the most suitable approach. (6 h. TYPE C) 3.2.- Design of a medium-complexity digital system in synthesisable VHDL. (6 h. TYPE B) 3.3.- Oral presentation. (1 h. TYPE C)

Planning

	Class hours	Hours outside the classroom	Total hours
Master Session	4	8	12
Integrated methodologies	15	31.5	46.5
Laboratory practises	6	7.5	13.5
Integrated methodologies	14	51	65
Presentations / exhibitions	1	8	9
Introductory activities	2	2	4

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Master Session	Conventional lectures. Through this methodology the outcome CE62/OP5 is developed.
Integrated methodologies	Problem based learning (PBL): Problem solving. Design of non- synthesisable models and synthesisable circuits in VHDL. To solve them, the student has to previously develop certain outcomes. Through this methodology the outcomes CG9, CG13 and CE62/OP5 are developed.
Laboratory practises	VHDL design of digital circuits and circuit implementation in FPGAs. Through this methodology the outcomes CG9, CG13 and CE62/OP5 are developed.
Integrated methodologies	Project based learning. The students must design a digital system in VHDL to solve a problem. In order to that, the students must plan, design and implement the necessary steps. The project development will be implemented in laboratory hours (type B). Besides, in type C hours there will be discussions and one-to-one interaction with the teacher. Activities to develop in the groups C: Analysis and debate about the project approach and different alternatives. Analysis and follow-up of the proposed solution. Design implementation. Analysis and debate of results. Oral presentations of the project results. Through this methodology the outcomes CG1, CG9, CG13 and CE62/OP5 are developed.
Presentations / exhibitions	Presentations/exhibitions: Exhibition of the results of the project developed. Through this methodology the outcomes CG1 and CG9 are developed.
Introductory activities	Introduction to the subject key topics both theoretical and practical. Through this methodology the outcomes CG13 and CE62/OP5 are developed.

Personalized attention

Methodologies	Description
Integrated methodologies	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Laboratory practises	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Integrated methodologies	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.

Assessment

	Description	Qualification	Training and Learning Results

Integrated methodologies	Resolution of theoretical problems and exercises. The majority of them will be focused on the design of non-synthesisable models and synthesisable circuits in VHDL. The problems will be based on the theoretical topcis. It will be necessary to teach to the professor the operation of each one of the models and circuits. The correct application of the theoretical concepts to the problems will be assessed, based on the published criteria. It will be necessary to deliver the documentation requested by the professor for each one of the exercises. Through this methodology the outcomes CG9, CG13 and CE62/OP5 are assessed.	50	B13	C62	
Integrated methodologies	Laboratory Project. Design of a medium-complexity synthesisable digital system in VHDL. It will be necessary to deliver the design source files. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria. Through this methodology the outcomes CG1, CG9, CG13 and CE62/OP5 are assessed.	40	B1 B9 B13	C62	D4
Presentations / exhibitions	It will be necessary to do an oral presentation of 15 minutes as a maximum about the work, according to the index supplied by the teacher. Through this methodology the outcomes CG1 and CG9 are assessed.	10	B1 B9		D4

Other comments on the Evaluation

The total mark will be the sum of the marks obtained in the different tasks of the subject.

The global mark of the theoretical problems has to be equal or greater than 5 over 10 in order to pass the subject.

The mark of the Laboratory Project has to be equal or greater than 5 over 10 in order to pass the subject.

All the students, both those who follow the subject continuously and those who want to be assessed in the final exam at the end of the term or at the end of the year (second opportunity), will have to do the tasks described in the previous section.

The students that do not attend classes regularly will also have to do the same tasks as the students who attend classes.

The final mark will be expressed in numerical form ranging from 0 to 10, according to the valid regulation (Royal decree 1125/2003 of 5 September; BOE 18 September).

Following the guidelines of the degree the students will be offered two assessment systems: continuous assessment and final assessment at the end of the term.

CONTINUOUS ASSESSMENT:

The students are considered to have chosen the continuous assessment when they have done 2 laboratory practices and/or 2 reports of theoretical exercises.

The students that have chosen continuous assessment, but do not pass the course, will have to do the final assessment at the end of the year.

The students that pass the course by means of continuous assessment will not be allowed to repeat any task in the final assessment in order to improve the mark.

The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the continuous assessment.

The students will develop the theoretical exercises and the laboratory practices individually.

The laboratory projects will be developed in groups of two students during the continuous assessment but the students will be assessed individually. To achieve this, the students will be required to explain during the oral presentation which parts of the project each of them has developed.

The students who want to be assessed in the continuous assessment can only miss two sessions as a maximum. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

FINAL ASSESSMENT:

The students that opt for the final assessment will have to do all the theoretical and practical tasks and the project individually.

The tasks for the final assessment have to be delivered before the official date of the examination set by the faculty.

In case the students pass the theoretical exercises (TE) and the Laboratory Project (LP), that is, the mark of each part >= 5,

the final mark (FM) will be the weighted sum of the marks of each part of the subject:

FM = 0'50 * TE + 0'40 * LP + 0'10 * OP

In case the students do not pass any of the two main parts of the subject, the theoretical exercises (TE) or the Laboratory Project (LP), that is, the mark of any task < 5, the final mark (FM) will be:

FM = Minimum [4'5; (FM = 0'50 * TE + 0'40 * LP + 0'10 * OP)]

Where:

TE = Global mark of the theoretical exercises and problems.

LP = Laboratory Project.

OP = Oral presentation.

ASSESSMENT CRITERIA.

1) Theoretical exercises and problems.

Each one of the theoretical exercises and problems proposed in the theoretical sessions will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of exercises assigned.

There will be eight reports of exercises.

The majority of the exercises will consist in the design of non-synthesisable models and synthesisable circuits in VHDL.

The assessment criteria are the following:

1. Correct design (CORR).

a. Behavioural model adequate to the project specifications.

b. Synchronous design.

c. Reusable design.

2. Functionality (FUNC). For each one of the exercises, the behavioural circuit model has to work perfectly to obtain the maximum mark. If the circuit is synthesisable, the temporary simulation of the resultant circuit also has to work perfectly.

a. Behavioural simulation.

b. Synthesis.

c. Timing simulation.

3. Project documentation (DOC).

a. Design source files.

b.Enough comments in the VHDL files to explain the sentences used.

It will be necessary to deliver the required source files.

The total mark will be the sum of the marks of each one of the exercise reports divided by the number of reports:

TE = (Report 1 + □ + Report 8) / 8

2) Laboratory Project.

This project consists in the design of a synthesisable digital system of medium complexity in VHDL.

The assessment criteria are the following:

1. Correct design (CORR).

a. System entirely synthesisable.

b. Suitable hierarchy arrangement.

c. Design totally synchronous.

d. Technology independent design.

e. Reusable design.

2. Analysis of the design and the implementation in FPGAs (ANA).

a. Analysis of the FPGA logical resources used and their justification.

b. Analysis of the internal system delays.

c. Analysis of the chosen implementation options.

d. Optimal utilisation of the FPGA logical resources.

e. Achievement of an optimal processing speed.

f. □Chipscope□ Verification.

3. Functionality (FUNC). For each circuit, the behavioral simulation, the timing simulation and the board test should work perfectly to obtain the maximum mark.

a. Individual circuits.

b. Complete system.

4. Documentation (DOC).

a. Design source files.

b. Enough comments in the VHDL files to explain the sentences used.

For the Laboratory Project (LP), it will be necessary to do an oral presentation.

3) Oral Presentation.

The assessment criteria are the following:

1. Clear structure and presentation order.

2. Clear explanations.

3. Enough explanations to understand the project.

4. Suitable figures.

Sources of information

Basic Bibliography

CHU, PONG P., **RTL Hardware Design Using VHDL: Coding for Efficiency,Portability, and Scalability**, John Wiley & Sons Inc, 2006

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Visión libros, 2013

Complementary Bibliography

ASHENDEN, PETER J., **The Designer's Guide to VHDL**, 3, MorganKaufmann Publishers, 2008

Standard IEEE VHDL Language Reference Manual (IEEE Srd 1076-2001), IEEE, 2001

CHU, PONG P., **FPGA Prototyping by VHDLExamples**, John Wiley & Sons Inc, 2008

Recommendations

Subjects that it is recommended to have taken before

Digital Electronics/V05G300V01402
Programmable Electronic Circuits/V05G300V01502

Other comments

The students will have previously followed the subjects Digital Electronics and Programmable Electronic Circuits. They give the necessary knowledge to understand the topics of this course.
It is not necessary to have passed them.
The students of the specialisation Electronic Systems, should have previously followed the subject Electronic Systems of Processed of Signal, but is not indispensable.