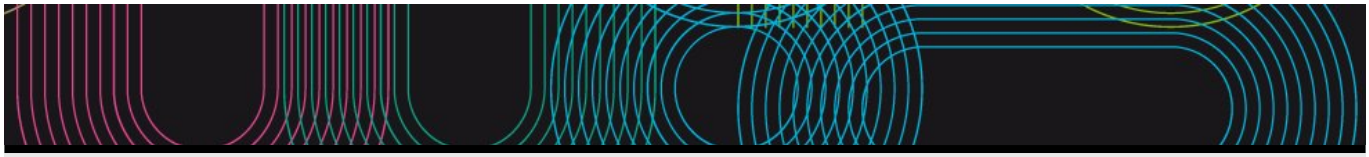

IDENTIFYING DATA				
Data Acquisition Systems				
Subject	Data Acquisition Systems			
Code	V05G300V01521			
Study programme	(*)Grao en Enxeñaría de Tecnoloxías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	3rd	1st
Teaching language	Spanish			
Department				
Coordinator	Río Vázquez, Alfredo del			
Lecturers	Río Vázquez, Alfredo del			
E-mail	ario@uvigo.es			
Web	http://webs.uvigo.es/ario/docencia/sad/sad.htm			
General description	This subject is about acquisition data, including instrumention amplifiers, analog switches, S&H and converters.			

Competencies	
Code	
A52	(CE43/SE5): The ability to design analogical and digital electronics circuits of analogical to digital conversion and vice versa, of radiofrequency, of feeding and electrical energy conversion for computing and telecommunication engineering.
A54	(CE45/SE7): The ability to design interface, data capturing and storage devices, and terminals for services and telecommunication systems.

Learning aims	
Expected results from this subject	Training and Learning Results
Knowledge of instrumentation amplifiers, and control about its use.	A52 A54
Knowledge of the different types of electronic analogue switches and the control of applications.	A52 A54
Knowledge of Sample&Hold circuits and their applications in data acquisition.	A52 A54
Knowledge of the operation of different DAC and ADC converters, and the control of their applications.	A52 A54
Knowledge about data storage and the control of their applications.	A52 A54
Knowledge of the design of data acquisition using the previous elements.	A52 A54

Contents	
Topic	
Analogue signals adaption	Analog multiplexers Digitally controlled amplifiers an basic attenuators
Galvanic isolation	Inductive isolation Capacitive isolation Optical isolation

Sample and hold	Sample and hold circuits Anti-alias filters
DACs I	DAC based on a multiplexer and a linear resistive network Digital potentiometers Switching DAC with weighting resistors
DACs II	Unipolar DAC with an R/2R network, in current mode. Unipolar DAC with an R/2R network, in voltage mode.
DACs III	Bipolar DACs. Indirect operation DACs.
ADCs I	Flash ADC. Half-flash ADC (sub-ranging)
ADCs II	Single-slope analogue ADC. Dual-slope analogue ADC. ADC based on successive aproximation register (SAR).
ADCs III	ADC based on a voltage-controlled oscillator (VCO) and a frequency-meter. ADC based on sigma-delta.
ADCs IV	ADC based on switching capacitors. Other applications based on switching capacitors.
Lab work 1	The instrumentation amplifier. Analogue multiplexer.
Lab work 2	Galvanic isolation amplifier. Optical coupler.
Lab work 3	Anti-alias filter. Sample and hold circuits.
Lab work 4	DACs based on R/2R network. Voltage mode. Current mode.
Lab work 5	Dual-slope ADC. Operational in bipolar mode.
Lab work 6	ADC using successive aproximation register (SAR). SAR based on software.

Planning			
	Class hours	Hours outside the classroom	Total hours
Troubleshooting and / or exercises	4	22.5	26.5
Tutored works	7	20	27
Laboratory practises	12	38	50
Master Session	15	27.5	42.5
Short answer tests	0.5	0	0.5
Troubleshooting and / or exercises	1	0	1
Short answer tests	0.5	0	0.5
Troubleshooting and / or exercises	1	0	1
Practical tests, real task execution and / or simulated.	1	0	1
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Troubleshooting and / or exercises	The lecturer will solve some exercises related to the subject. Competencies A52 and A54 will be addressed in these sessions.
Tutored works	The lecturer will lead the students in a data acquisition system design. Competencies A52 and A54 will be addressed in these sessions.
Laboratory practises	Simulations and real assembled circuits will be tested. Competencies A52 and A54 will be addressed in these sessions.
Master Session	The lecturer will show some theoretical contents related to the subject. Competencies A52 and A54 will be addressed in these sessions.

Personalized attention	
Methodologies	**Description**
Master Session	Students are permitted to interrupt the session in order to ask the lecturer for some doubt related to the session.

Troubleshooting and / or exercises	Students are permitted to interrupt the session in order to ask the lecturer for some doubt related to the session.
Tutored works	Students are permitted to interrupt the session in order to ask the lecturer for some doubt related to the session.
Laboratory practises	Students are permitted to interrupt the session in order to ask the lecturer for some doubt related to the session.

Assessment

	Description	Qualification
Tutored works	Every student has to write a document related to the asigned work. Competencies A52 and A54 will be assessed in these works.	10
Short answer tests	First short answer test, in the classroom. Competencies A52 and A54 will be assessed in these tests.	15
Troubleshooting and / or exercises	First exercise test, in the classroom. Competencies A52 and A54 will be assessed in this test.	15
Short answer tests	Second short answer test. Competencies A52 and A54 will be assessed in this test.	15
Troubleshooting and / or exercises	Second exercise test. Competencies A52 and A54 will be assessed in this test.	15
Practical tests, real task execution and / or simulated.	Laboratory-work exam based on simulations and real circuits. Competencies A52 and A54 will be assessed in this test.	30

Other comments on the Evaluation

NOTE: The timing of the partial exams might suffer some changes, due to time restrictions. The exact timing will be indicated along the course.

CONTINUOUS EVALUATION OPTION:

The subject is evaluated in a continue way, by mean of two partial exams. These exams treat the theoretical aspects. In addition, there is an exam for the lab-work.

This first partial includes themes from one to five. The second partial exam includes themes from six to ten. The weight of both partials is a 60% from the total mark.

The two partials take place in the classroom, within the class time. These partials are approximately 90 minutes long. The first 30 minutes will be dedicated to an exam with short answers. The rest 60 minutes will be dedicated to an exam with long answers.

Inside each partial, the 90 minutes exam and the 30 minutes exam have the same weight.

In order to pass a partial exam (the first or the second), the student is required to obtain at least a mark of 5 over 10.

The student that passes only one partial will only have to try the other one at the final exam option.

The lab-work is evaluated using a unique exam, in the laboratory. The weight is 30%.

Tutored works are assessed using a report that every student should be done. The weight is 10%.

When a student attends the first partial, he or she accepts to follow the continuous assessment. Students that do not attend to the first partial will be assessed by means of a final exam.

The mark that a student obtains in the lab-work is maintained until July, except if the student does not want. In this case, the student will have to do partials and lab exams in July.

In order to pass the subject, once partials have been passed, the student has to obtain a global mark (GM) of at least 5 points in ten. The global mark is calculated following the next formula:

GM = 0.6 * TM + 0.3*LM + 0.1*RM

where

TM = Mean value of the partial marks; LM = lab mark; RM = report mark

The first partial is preview to take place in the sixth week. The second partial will take place in the last week.

The lab exam will take place in the lab, the day of the last lab session.

FINAL EXAM OPTION:

The students that do not follow the continuous assessment will be assessed by means of a final exam. The exam will consist of three parts: the first part of the themes 1 to 5, the second part of the themes 6 to 10 and the third part of lab-work in the laboratory.

In order to pass the subject, the student has to obtain a mark of at least 5 points over ten for the first and second parts. In this case, the global mark (GM) is calculated following the next formulae:

GM = 0.6 * TM + 0.4*LM

where:

TM = Average mark of the first and second part of the exam; LM = lab mark

If the student does not obtain a mark of at least 5 in the first part or in the second part, the global mark would be the least mark between 4 or the GM taken from the early formulae.

IMPORTANT:

If a student did not enter the continuous assessment mode but is interested in participate in the final exam, he or she should talk with the professor at least two weeks before the day of the exam. Contact can be by e-mail. This way, the organization of the lab-work exam will be simpler.

RECOVERY EXAM

The recovery exam (June-July) shares the same structure than the final exam.

Sources of information

Paul Horowitz y Winfield Hill, **The Art of Electronics**, Cambridge Univ. Press.,

Sergio Franco, **Design with Operational Amplifiers and Analog Integrated Circuits**, WCB/McGraw-Hill,

Franco Maloberti, **Data Converters**, ISBN 978-0-387-32485-2,

Analog Devices Library,
hhtp;//www.analog.com/library/analogDialogue/archives/43-09/EDCh%206%20Converter.pdf, Capitulos 6.1,6.2,6.3,

Recommendations

Subjects that continue the syllabus

Analogue Electronics/V05G300V01624

Subjects that are recommended to be taken simultaneously

Analogue Electronics/V05G300V01624

Subjects that it is recommended to have taken before

Electronic Technology/V05G300V01401

Other comments

I recommend the students to search the web for information about this subject. Electronic devices factories show interesting information. Many universities around the world hung interesting notes in the Internet. And many of them for free.